REMARKS

This amendment is responsive to the Final Office Action dated June 6, 2005. Claims 21 - 58 are pending in this application and have been rejected. The Examiner has that Claims 22 - 23, 28 - 32, 33 - 34, 39, 44 - 46, 48 - 50, 53 and 58 would be allowable rewritten to overcome rejections under 35 USC § 112 (second paragraph). Applicant has, therefore, canceled all other claims where prior art rejections have been applied

Applicant has amended this application to overcome § 112 rejections in claims that are considered to be allowable at the top of page 7 of the outstanding Office Action.

In claim 21, Applicant has amended the claim to relate the inputs to each channel. Figures 2 and 12 show an input to amplifier (52) (Figure 2) or amplifier (90) (Figure 12). Applicant has deleted the language "at least one amplifier selected from said plurality of amplifiers" in response to the rejection.

In claim 33, Applicant has amended the claim to refer to a circuit connected to an output of the peak and hold or sample and hold and recited the multiplexing to the output circuit system previously recited in claim 21.

In claim 39, Applicant has amended the claim to read a

"process signal" which is the function of the circuitry shown in Figure 2. Processing is recited in claim 21 as noted by the Examiner.

In claim 46, Applicant has amended the claim in order to recite the time difference measurement circuit connected to the output circuit system. The time difference measurement circuit is found in Applicant's Figure 12 and described at page 28, line 40 as well as at page 11, lines 27 - 28 and page 16, line 3.

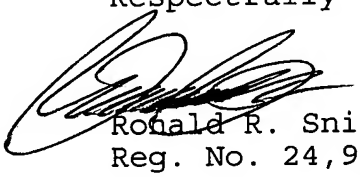
Claim 49 has not been amended because it is believed to be clear. The language "at least one" of the plurality of comparators is a discriminator. The claim merely states that one is discriminator and does not state that the plurality of comparators is a single comparator. The claim is interpreted as one of the plurality of comparators being a discriminator type.

Claim 53 has not been amended. Claim 53 is supported by the Abstract, line 3, and the specification at page 7, line 12, page 12, line 16, page 28, line 25, page 29, line 16, and page 33, line 5. At page 12, lines 16 - 19, it is stated that "there is also a pole-zero circuit after input amplifier (52) or anywhere else in the chain if better, not shown. The pole zero circuit can be switched on or off as necessary. Pole zero circuit reduces the pile up effect and thus increases the ASIC throughput rate." In this description, Applicant places the pole zero circuit down stream from amplifier (52), which is shown in Figure 2. Claim 53 has been amended to recite a pole zero circuit as

it is stated in the specification.

In view of the foregoing, it is respectfully submitted that the application is now in condition for allowance, and early action in accordance thereof is requested. In the event there is any reason why the application cannot be allowed in this current condition, it is respectfully requested that the Examiner contact the undersigned at the number listed below to resolve any problems by Interview or Examiner's Amendment.

Respectfully submitted,



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